# Getting Started with SystemVision™

Software Version 4.4

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# Chapter 1
# Overview

SystemVision™ provides co-simulation capability for mixed-signal designs consisting of analog and digital models. SystemVision integrates the design processing of DxDesigner™ with the ADVance MS™ mixed-signal simulator along with its own waveform analyzer as a single simulation, analysis, and verification tool. Models and modeling techniques from VHDL-AMS, VHDL, C, and Eldo® SPICE simulation environments are supported.

This manual provides basic information on how to begin using SystemVision. As you use this information, feel free to experiment with product features and functions not explicitly covered. If you want to begin trying out SystemVision right away, skip to the examples in Chapter 2, "Simulating an Existing Design" and Chapter 3, "Creating and Simulating a New Design". These examples show how to create a simple design, simulate it, and view the results.

The rest of this chapter consists of the following sections:


- Background Information
- How to Invoke SystemVision
- Basic Terms
- User Interface


## Related Documents

### Online Help

In SystemVision or in the waveform analyzer, you can display online help as follows:

- For SystemVision, select **Help > SystemVision Help** from the main menu. Help is displayed as HTML in a browser window.
- For the waveform analyzer, select **Help > Contents and Index** from the main menu. Help is displayed in JavaHelp format.

### Manuals

You can access the following manuals using the **Help > SystemVision** command:

- *SystemVision User's Manual* contains introductory information on how to use the SystemVision simulation environment.

- *SystemVision Simulator User's Guide* contains usage and reference information on the mixed-signal, mixed language SystemVision simulator for SPICE and VHDL-AMS.

## Supplemental Materials

*The System Designer's Guide to VHDL-AMS: Analog, Mixed-Signal, and Mixed-Technology Modeling* by Peter Ashenden, Gregory Peterson, and Darrell Teegarden is a book published by Morgan Kaufmann Publishers (ISBN 1558607498). It is a follow-up to Ashenden's *The Designer's Guide to VHDL* and contains information on the syntax and semantics of the VHDL-AMS modeling language. The book also provides techniques and examples on using VHDL-AMS to model both electronic and non-electronic systems.

In particular, the following chapters contain case studies (examples) that were developed using ADVance MS and VHDL-AMS:

- Chapter 8—*Case Study 1: Mixed-Signal Focus*
- Chapter 14—*Case Study 2: Mixed-Technology Focus*
- Chapter 18—*Case Study 3: DC-DC Power Converter*
- Chapter 23—*Case Study 4: Communication System*
- Chapter 26—*Case Study 5: RC Airplane System*

For more information on this book, refer to the following website for Morgan Kaufmann Publishing:

http://www.mkp.com/vhdl-ams

## Release Notes

Release Notes for SystemVision are provided in HTML format at the following location:

***sv_install***`\readme_sv.htm`

where *sv_install* is C:\mentorgraphics\SystemVision4.4 or the directory where you installed SystemVision.

You can also refer to the SystemVision website for the latest product information:

http://www.mentor.com/systemvision/

# Background Information

## AMS Means “Analog Mixed-Signal”

Because SystemVision supports the VHDL-AMS modeling language, that means you can write or use models for technologies that are not necessarily electrical. The analog extensions specified by IEEE Std. VHDL 1076.1-1999 enable you to use simulation models that characterize continuous behavior based on differential algebraic equations (DAEs). Using a hardware description language such as VHDL-AMS as part of design simulation is sometimes referred to as *math-based computer-aided prototyping*.

SystemVision can simulate VHDL-AMS models and designs with the following features:

- Non-electrical domains (such as magnetic, thermal, mechanical, hydraulic)
- Analog (continuous-time) and digital (event-driven) models in the same design
- Initial conditions
- Piecewise-defined behavior
- Small-signal frequency domain specifications
- Noise
- Transfer functions
- Existing SPICE models

## Configuration Requirements

Table 1-1 lists the operating systems supported for this release of SystemVision, along with minimum hardware requirements.

**Table 1-1. Minimum Requirements for SystemVision**

| OS | CPU | RAM | Disk Space |
|---|---|---|---|
| Windows XP<br>Windows 2000 | Pentium-class, 500 MHz | 512 MB | 700 MB |

## Licensed Versions

This release of SystemVision is provided in three versions, Professional, Electrical/Electronic, and Educational. The versions differ by their price and the limitations to their respective design sizes. The Educational version is directed toward technical education programs at colleges and universities and toward entry-level applications in the EDA industry.

The following functionality is included in the Professional version of SystemVision, and is available for the Electrical/Electronic version with a separate license:

- Simulator Multi-run analyses:
  - Parametric Sweep, DC Sweep
  - Monte Carlo
  - Sensitivity
  - Worst-case analysis
- Waveform viewer multi-run analyses:
  - Calculator operations on multi-run data
  - Waveform Measurements on multi-run data

Note that the license for the Educational version is node-locked and can only be used on the computer whose hostID is given in the license.

# Limitations and Conditions

## Design size

The license for each version restricts the design size for simulation to the following maximum limits:

| | Educational | Electrical/Electronic | Professional |
|---|---|---|---|
| VHDL-AMS Analog quantities | 30 | 100 | 1500 |
| SPICE Analog nodes | 30 | 1500 | 1500 |
| Digital signals | 100 | 300 | 3000 |

## Not supported for this release

The following features and capabilities are not available in SystemVision for this release:

- UNIX platforms (Sun or Hewlett-Packard)
- Packaging capability to PCB layout
- Verilog language

# Libraries and Symbols

SystemVision provides both a model library (Educational Library - edulib) and a symbol library for design elements in your schematic. This release of SystemVision supports simulation and analysis of VHDL-AMS and SPICE models only. It is not intended to work with other board design products in the DxDesigner environment.

## Symbol Libraries

The SystemVision application provides libraries for symbols in the following location:

```
sim\systemvision\SymbolLibs
```

where sv_install is C:\mentorgraphics\SystemVision4.4 or the installation directory you designated for SystemVision.

This directory contains the following library subdirectories, each of which provides a variety of symbols that you can place on a schematic.

| | | |
|---|---|---|
| ControlSystems | Magnetic | SpicePrimitive |
| Digital | MixedSignal | SpiceSemiconductor |
| Electrical | MixedTechnology | Thermal |
| Hydraulic | Rotational | Translational |
| SpiceMacromodel | Fundamentals_VDA | Megma_VDA |
| SVX | Spice2VDH_VDA | |

Except for the symbols in SpicePrimitive, SpiceSemiconductor and SpiceMacroModel libraries, each symbol has a VHDL-AMS model assigned to it. Fundamentals_VDA and Spice2VHD are provided by VDA.

## Model Libraries

The SystemVision application provides libraries for the models listed below in the following locations:

```
sv_install\sim\win32\edulib\v4.4_1.1
```

where sv_install is C:\mentorgraphics\SystemVision4.4 or the installation directory you designated for SystemVision.

This collection of VHDL-AMS models is referred to as the Educational Library (edulib) and is partitioned into the following categories:

| | | |
|---|---|---|
| ControlSystems | Magnetic | Thermal |

| | | |
|---|---|---|
| Digital | MixedSignal | Translational |
| Electrical | MixedTechnology | |
| Hydraulic | Rotational | |

These libraries are listed under Model Libraries of the **Simulation** tab in the Project Navigator.

A set of SPICE component libraries are available at the location:

```
sv_install\sim\SpiceComponentLibs
```

where *sv_install* is C:\mentorgraphics\SystemVision4.4 or the installation directory you designated for SystemVision.

The SPICE component libraries are only available in the Professional version of SystemVision. They can be accessed either through DxDataBook or added individually to the Spice Libraries node under Model Libraries of the **Simulation** tab in the Project Navigator.

To add a SPICE Library:

1. Select the **Simulation** tab in the Project Navigator.
2. Click [+] next to Model Libraries.
3. Right-click Spice Libraries and select Add Spice Library.
4. Navigate to and select the library you need to add, then click **Open** in the Select a Spice library dialog box.

The VDA Automotive Development component library is located in the following location:

```
sv_install\sim\systemvision\win32\Libraries
```

where *sv_install* is C:\mentorgraphics\SystemVision4.4 or the installation directory you designated for SystemVision.

# Online Help

## SystemVision

The online help for SystemVision provides context-sensitive information on its features and functions. You can display the name about each icon in the toolbar by moving the mouse cursor over it.

You can display the online help for SystemVision by choosing **Help > SystemVision Help** from the menu bar of the main application window (see Figure 1-1).

## Waveform Analyzer

The waveform analyzer for SystemVision is a separate application that contains its own online help. The contents and topics apply only to using the waveform analyzer. You can display the online help for the waveform analyzer by choosing **Help > Contents and Index** from the menu bar of the Waveform Analyzer window.

# How to Invoke SystemVision

When you install SystemVision, the installation program creates two ways to invoke SystemVision:

- The Windows Start menu

  **Start > Programs > Mentor Graphics SystemVision > SystemVision**

- The desktop icon

  Double-click the SystemVision icon.

# Basic Terms

The following terms apply to the way SystemVision manages design information.

- **Design** — a network of models (usually represented by a schematic or structural HDL code) that can be simulated by SystemVision.
- **Block** — a design that can be used as part of a larger design.

**Note**

This meaning of the word block is different from that of a block symbol or a functional block (fub) which is a type of symbol you can create.

- **Component** (Part) — a specific instance of a model within a design. A component could be displayed as multiple symbols on a schematic. For example, an op amp component could consist of models of other discrete components, such as transistors and resistors.
- **Primitive** — the lowest level of a model, with no dependencies on other models for its definition.
- **Design hierarchy** — an ordered listing of the components used in a given design.
- **Net** — the connection between two or more models.
- **Node** — an intersection of nets.

- **Attribute** — a language-dependent characteristic of an element (such as a model or netlist) that takes a user-specified value. The value must be specified in the language used to define the element.
- **Symbol** — the graphical representation of a model.
- **Functional block** (fub) — a DxDesigner user-defined symbol. When you create a fub, you must associate it with a model. You can also assign it to a library, if desired.
- **Pin** — the connection point of a component symbol.
- **Property** — a characteristic of a model or symbol that takes a user-specified value.
- **Parameter** — a characteristic of a model or symbol that takes a user-specified value.
- **Library** — a collection of files that contain symbol definitions or model definitions (such as files containing VHDL-AMS models).
- **Schematic** — the graphical display of symbols and connections that represent a design. The schematic for a design is saved as a file in a project.
- **Sheet** — the extension of a schematic (also referred to as a page). If you have large schematic that does not fit into the document display area of SystemVision, you can partition it into multiple sheets. Sheets do not necessarily create hierarchy for the design (although you can create hierarchy on different sheets).
- **Wire** — the graphical connection between two or more symbols on a schematic.
- **Testbench** — a unique, operational design unit (schematic or HDL code) that consists of a netlist of model instances and settings for simulation. Every simulation is performed on a testbench. The design unit may or may not contain its own driving stimulus and loads for simulation. (As an HDL term, “testbench” is the stimulus that is affixed to the design for simulation purposes).
- **Experiment** — a unique collection of settings that you specify for a given simulation and the results of the simulation on a given design.
- **Project** — a working collection of designs, schematics, test benches, experiments, libraries, and associated files the application uses to manage data. You must use a project to operate on your design and save the results. When you save a project, information about the project contents is saved with the file extension .dproj.
- **Root** (Design Root) — a symbolic design associated with a specific testbench. Usually a schematic, the root is the top design entity in a hierarchical design that is under test. The root might or might not contain a driving stimulus that can produce results. Typically, a testbench is attached to the design root.
- **Database** —SystemVision uses the DxDesigner database structure to store project information such as connectivity, symbol data, and instance data. The results of a simulation is stored as a waveform database file with a .wdb extension.

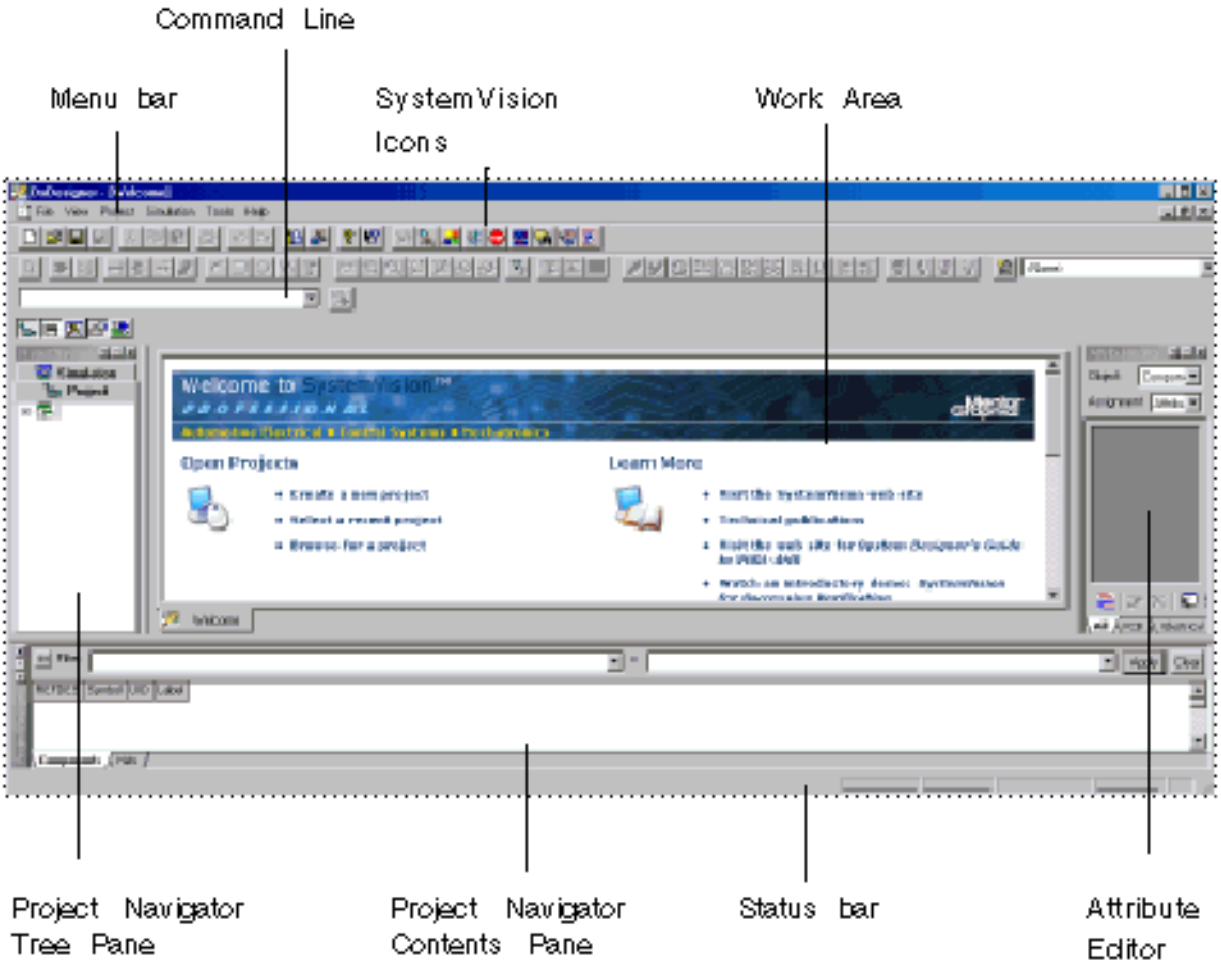
- **File** — the basic element of data storage. You can open, read, and write to any file, except a project file, when the project associated with that file is open.

# User Interface

## Main Window

Figure 1-1 shows the main window of the graphical user interface (GUI) that appears when you invoke SystemVision.

**Figure 1-1. Main Display Window**




This window is based on the DxDesigner GUI and contains the following features:

**Menu bar** — allows you to select pulldown menus for File, View, Project, Tools, Simulation, Window, and Help.

**Note**

For convenience, many of the actions provided in the menu bar are duplicated by popup menus, which you can display by clicking the right mouse button.

**Command line** — allows you to enter commands that apply to the design currently being displayed.

**Toolbar icons** — provide shortcuts for commonly used commands you can select from the main menu. Icon groups on toolbars are separated by blank space.

**Project Navigator (Tree Pane)** — displays information about your project in a hierarchical format. The following tabs at the top of the Work Area let you switch between the type of design information displayed:

- Project — Design Roots, Libraries, and Folders. These listings show the hierarchy of schematics, symbol libraries, and files associated with the current project.
- Simulation — Simulation, Analysis, and Results. These listings show the testbenches, model and work libraries, and result databases associated with the current simulation.

**Work Area** — the display area where you graphically create or view your design. When you initially invoke SystemVison, the Welcome Screen is in this pane; thereafter, project information such as the design schematic is displayed.

**Status bar** — provides real-time information on actions you perform in the working area.

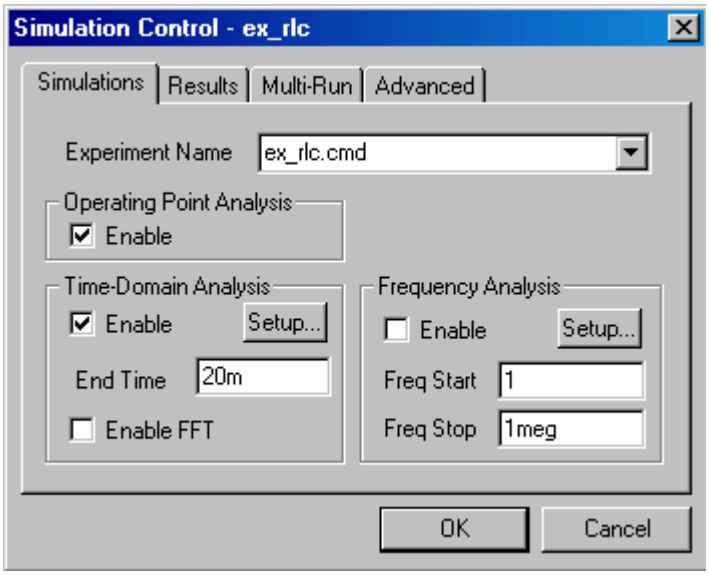
**Attribute Editor** — a listing of all the attributes for a selected component in the schematic. You can edit attributes by right-clicking on the component then and choosing Properties from the popup menu.

**Project Navigator (Contents Pane)** — a listing of the reference designator, symbol, and labels for all parts and nets in the current design.

## Simulation Control Dialog

In SystemVision, you control simulation using the Simulation Control dialog box shown in Figure 1-2. The dialog box provides tabbed panes; each pane enables you to specify the indicated simulation settings.

**Figure 1-2. Simulation Control Dialog Box**




**Simulations** — enables you to specify the types of analysis you want to perform.

**Results** — enables you to specify the signals you want to save for display in the waveform analyzer.

**Multi-Run** — enables you to specify settings for simulation sweeps (SPICE netlists only).

**Advanced** — enables you to specify simulation accuracy, time steps, and invocation arguments.

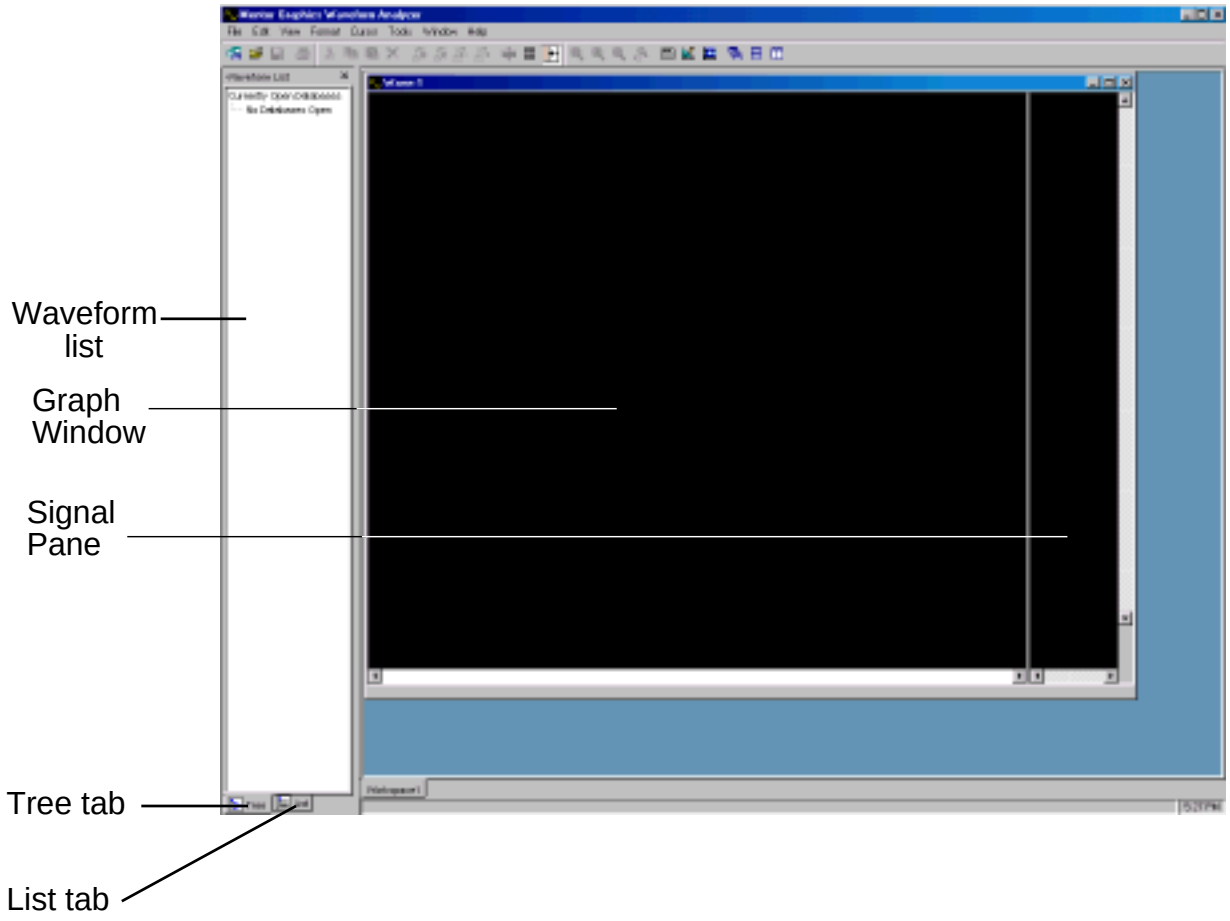
## Waveform Analyzer

Figure 1-3 shows the SystemVision waveform analyzer window.

The main display areas are:

- Waveform list — contains the names of the waveforms that you specified in the **Results** tab of the Simulation Control dialog box (see Figure 1-2). The bottom of this panel contains two tabs, which allow you to select the display format for these signal names:
  - **Tree** tab — lists signal names hierarchically (click the[ **+**] and [**-**] boxes to expand or collapse the listing).
  - **List** tab — lists all signal names without hierarchy (flat).
- Graph window — consists of the waveform display pane and the signal pane. The signal pane lists the name of each waveform in the waveform display pane.

**Figure 1-3. Waveform Analyzer Window**



# Chapter 2
# Simulating an Existing Design

## Introduction

This chapter explains how to run a simulation on an example that is included as part of the SystemVision installation. The design is a simple electrical circuit consisting of a resistor, inductor, and capacitor (RLC) model. The models are VHDL-AMS models from the Educational Library provided with SystemVision.

Exercise 1 guides you through:

- Opening an existing project
- Setting up and running a simulation
- Viewing the results of your simulation in the SystemVision waveform analyzer

For basic information on using SystemVision, refer to Chapter 1, "Overview".

**Note**

This example runs with either licensed version of SystemVision (Professional or Educational.

## Exercise 1: Simulate a Simple RLC Circuit

This exercise shows how to invoke SystemVision, open an existing design as a project, perform some basic operations, and explore the user interface.

### Set Up for Simulation

1. Invoke SystemVision.

   When you installed SystemVision, the installation program created an invocation shortcut in your Windows Start menu. To invoke SystemVision, select the following from the Start menu:

   **Start > Programs > Mentor Graphics SystemVision > SystemVision Professional**

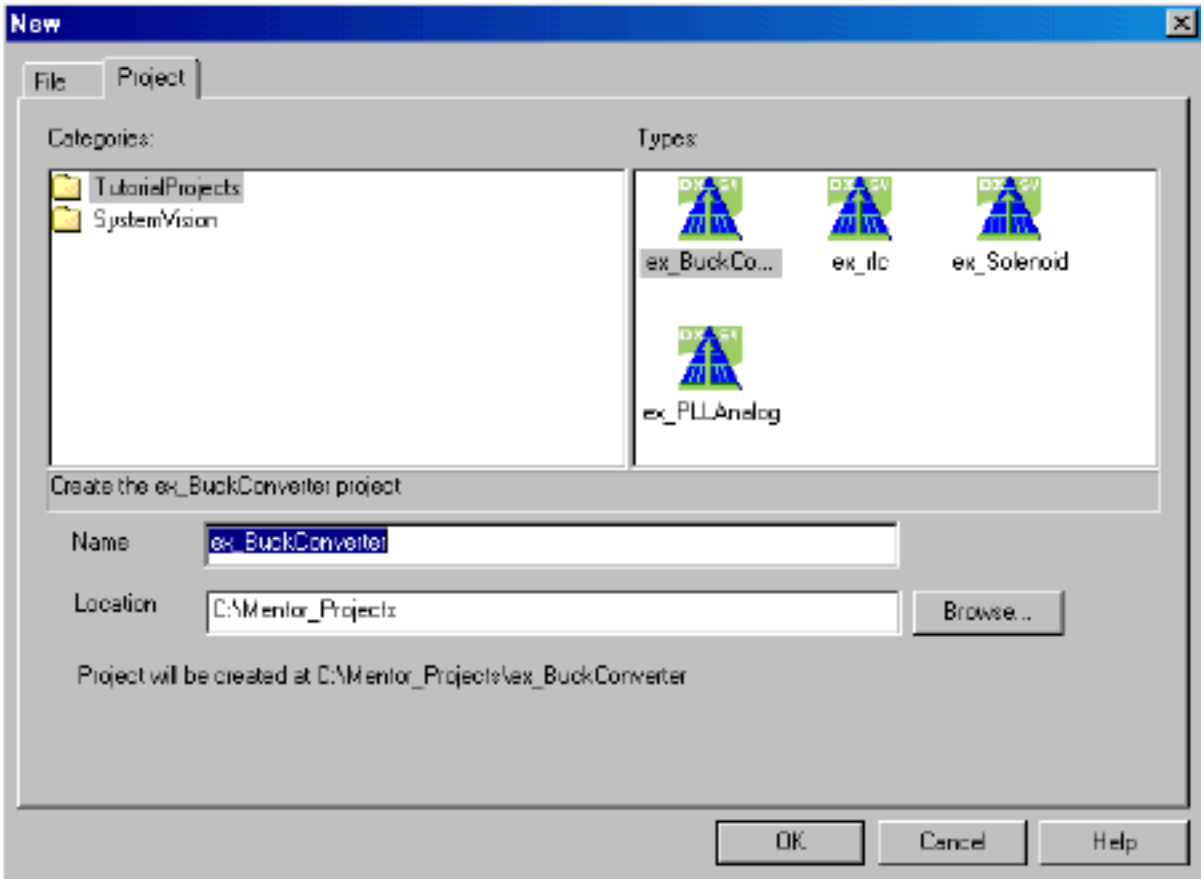
   If you are using the Educational version, substitute **SystemVision Educational** for **SystemVision Professional**.

   The main SystemVision window, as shown in Figure 1-1, in Chapter 1, is displayed.

2. Close the Hint dialog.

   The New Project dialog box shown in Figure 2-1 is displayed.

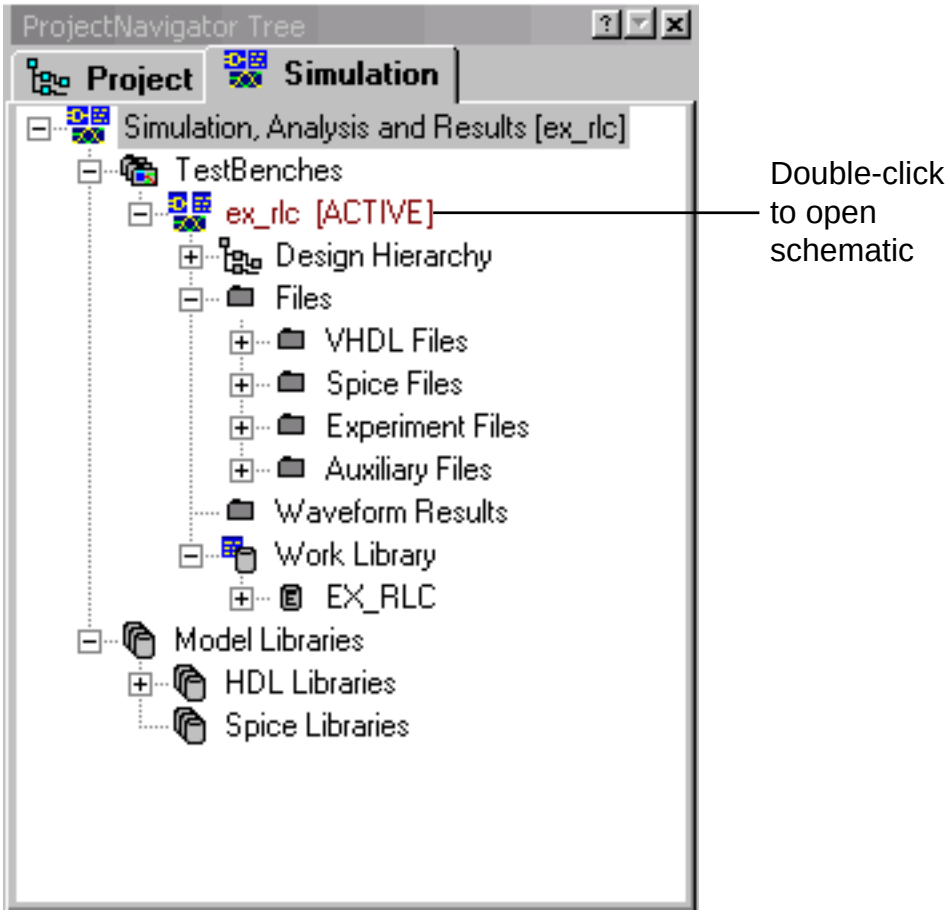
**Figure 2-1. New Project Dialog Box**




3. Select the resistor-inductor-capacitor (RLC) ex_rlc project.
4. Click **OK** to open the project.
5. Expand the project hierarchy.
   a. At the top of the Project Navigator (Tree pane), click the **Simulation** tab. Note the [+] indicator to the left of the TestBenches and Model Libraries for this project.
   b. Click the [+] next to TestBenches. The testbench listing is expanded and the contents of the testbench are displayed.
   c. Click the [+] next to Model Libraries. The available model libraries are displayed.
   d. Under TestBenches, click [+] next to ex_rlc [ACTIVE] then click [+] next to Files and Work Library.

      Figure 2-2 shows the listing of files associated with this testbench.

**Figure 2-2. Project Navigator Showing Design Hierarchy**



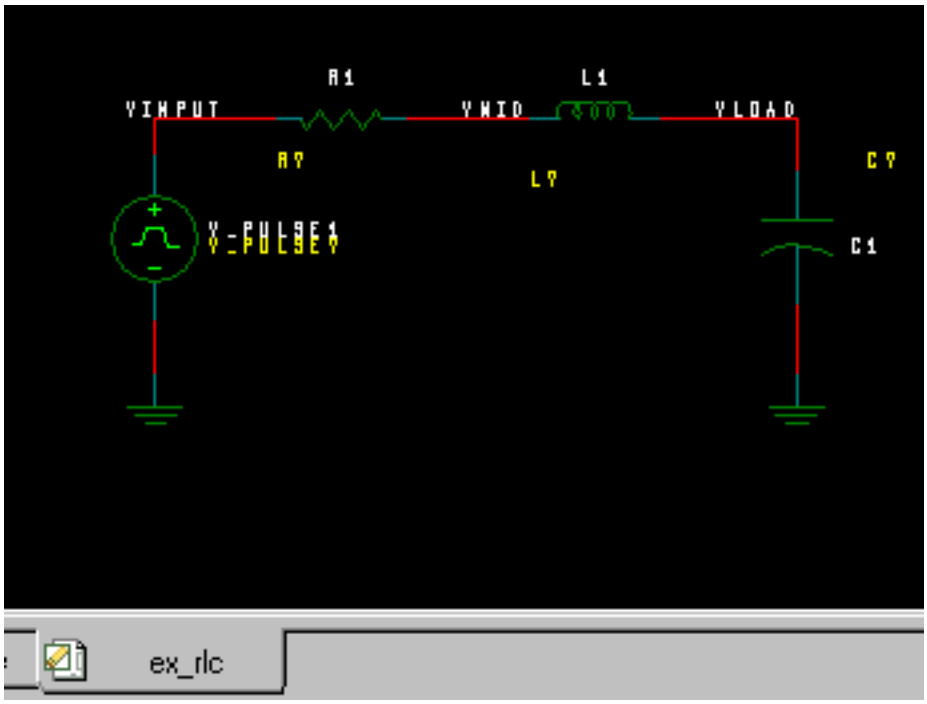

6. Open the schematic for this design.

   a. Under TestBenches, double-click ex_rlc, which displays the schematic for this design (see Figure 2-3).

   b. (Optional) Click the zoom icons in the View Toolbar to adjust the size of the display.

   c. (Optional) Right-click any component, such as R1 or C1, to display a popup menu and select **Edit Model Properties**. This displays the Model Properties dialog box, which lists the general and parameter values specified for the selected component.

**Figure 2-3. Schematic Display**




V1 = 5V R1 = 3Ω L1 = 1mH C1 = 10µF

**Note**

The **Netlist** and **Compile** commands (Steps 7 and 8 ) are automatically performed when you run the **Simulate** command. Alternatively, you can run either of these commands if you want to netlist or compile without simulating.

7. (Optional) Netlist the design.

   a. In the Project Navigator, select ex_rlc under TestBenches.

   b. Select **Simulation** > **Netlist** from the main menu.

      The netlist transcript is displayed in the **Simulation** tab of the Output Log pane. If the Output Log pane is not open, the application automatically opens the pane at the bottom of the main window with the **Simulation** tab active.

8. (Optional) Compile the testbench design.

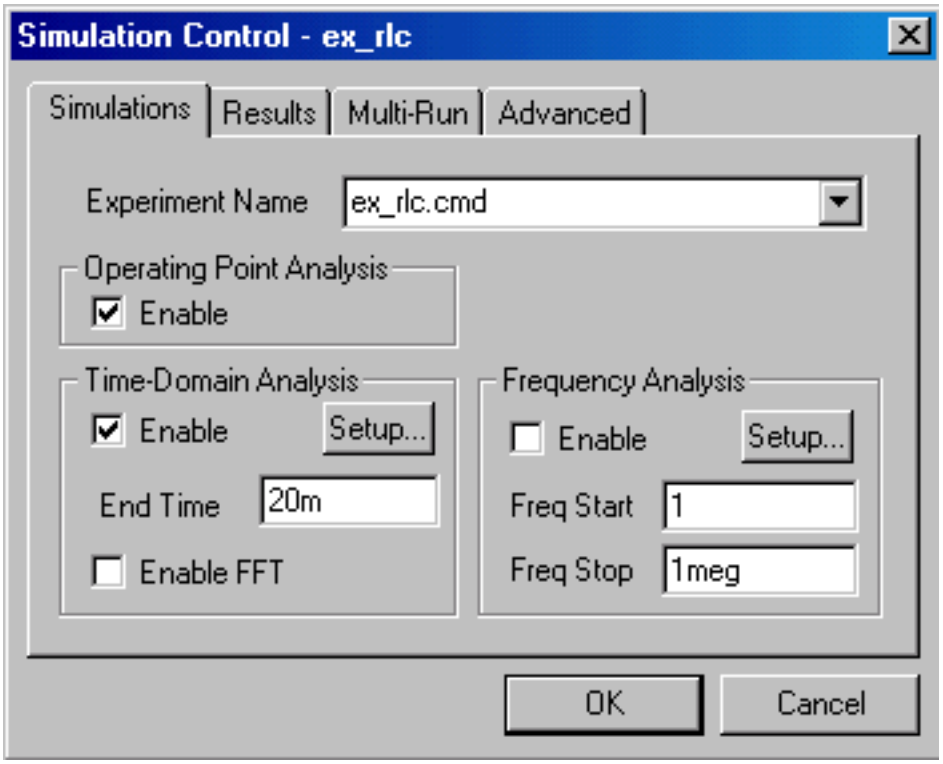
   Select **Simulation** > **Compile** > **Compile All** from the main menu. This compiles the active testbench and displays the progress of the compilation in the **Simulation** tab of the Output Log pane.

9. Specify the simulation settings.

   a. Select **Simulation** > **Simulate** from the menu bar. This displays the Simulation Control dialog box (see Figure 2-4), which provides four tabs: **Simulations**,

**Results**, **Multi-Run**, **Advanced**. When you click a different tab, the dialog box changes to provide different simulation settings.

**Figure 2-4. Simulation Control—Simulations Tab**




b. In the **Simulations** tab:

   i. Enable **Operating Point Analysis** and **Time-domain Waveforms**.

   ii. Under **Time-domain Waveforms**, enter the following value:

   End Time 20m

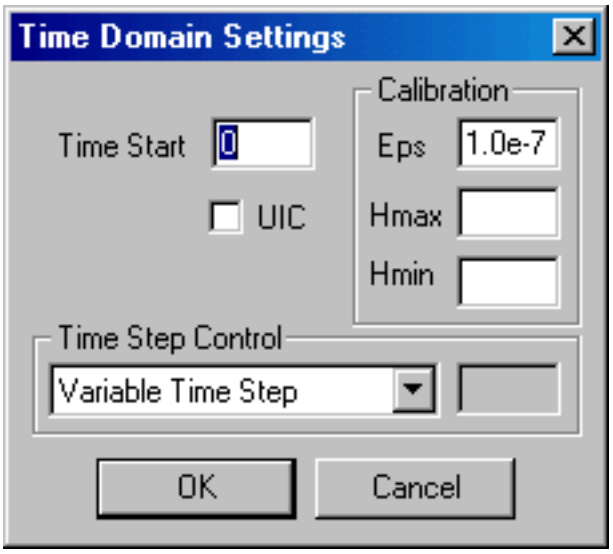
c. Click **Setup** to display the Time Domain Settings dialog box (Figure 2-5).

   i. Under **Calibration**, enter the following in the **Eps** field: 2.0e-7

   Eps is epsilon, the parameter for overall simulation accuracy.

   ii. Leave the values for **Hmin** (minimum time step) and **Hmax** (maximum time step) blank. Click **OK**.

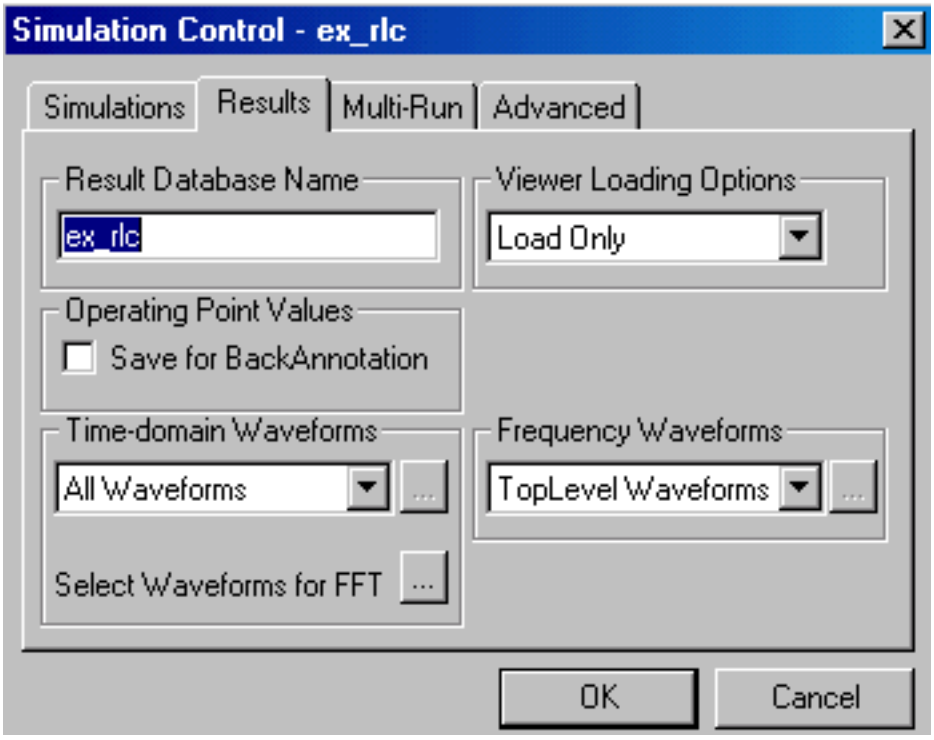
**Figure 2-5. Time Domain Settings**




10. Specify Results settings.

    a. Click the **Results** tab. Figure 2-6 shows the fields that specify which waveforms to display after simulation.

**Figure 2-6. Simulation Control—Results Tab**



i. Click the dropdown list under **Time-domain Waveforms** and select Selected Waveforms.

ii. Display the list of available waveforms to select by clicking the browse button next to the dropdown list:

iii. In the Select Time-Domain Waveforms dialog box, expand the r1, l1, c1, and v_pulse waveform listings then click **Clear All**.

iv. Select the check boxes for the following waveforms:

| | |
|---|---|
| V(vmid) | l1 - S[i] |
| V(vinput) | c1 - S[v] |
| V(vload) | c1 - S[i] |
| r1 - S[v] | v_pulse1 - S[v] |
| r1 - S[i] | v_pulse1 - S[i] |
| l1 - S[v] | |

v. Click **OK** to close the Select Time-Domain Waveforms dialog box.

# Run Simulation

## Time-domain analysis

1. Click **OK** to run the simulation for operating point and time domain analysis.

   Simulation of the active testbench (ex_rlc) shown in the Project Navigator is started.

   During simulation, the following types of analysis are performed:

   - Operating point analysis
   - Time domain analysis

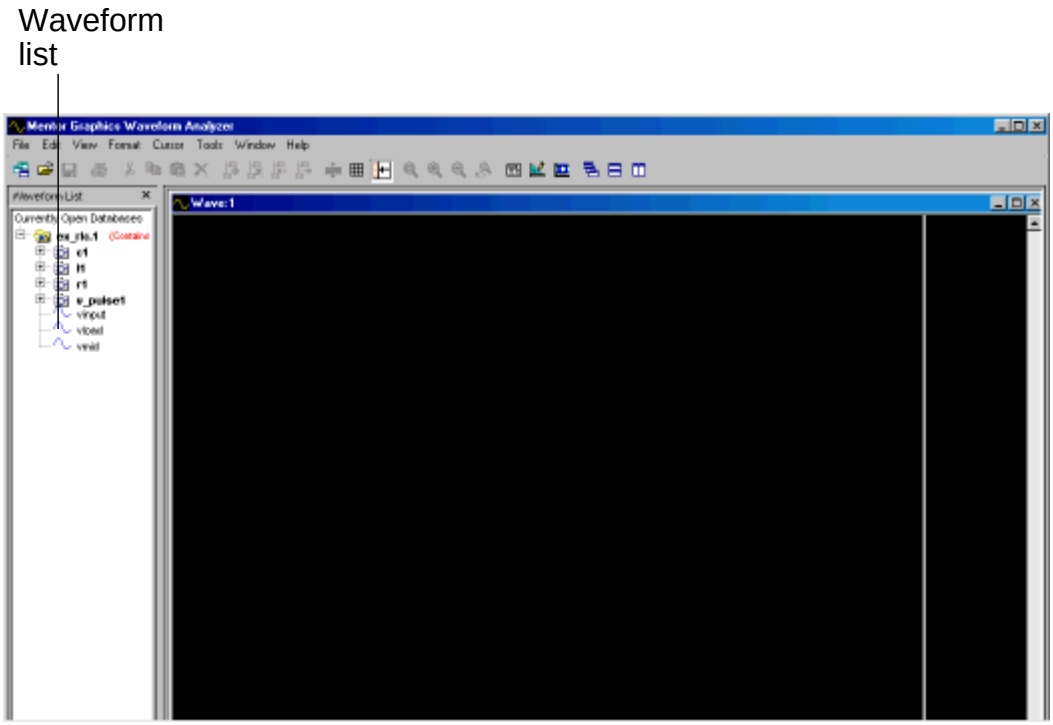
   Later, in "Frequency-domain analysis" on page 27, you will run a small-signal frequency analysis and view the results.

   When simulation is complete, SystemVision launches the waveform analyzer as shown in Figure 2-7. Note the waveform list, which shows a hierarchical list of signals for each design element in the testbench.

**Note**

The phrase "Contains unsaved changes" means that these waveforms are loaded into memory only—they have not been saved to your database. Step 3 describes how to save simulation results.

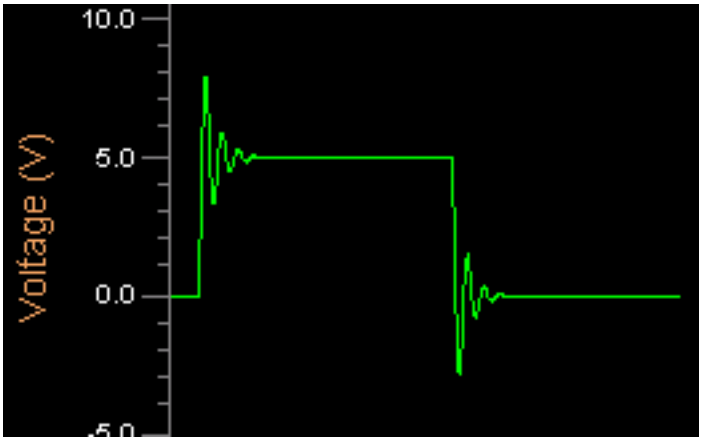
**Figure 2-7. SystemVision Waveform Analyzer**




2. View results of the time domain analysis.

   a. In the waveform list, double-click the vload signal. Figure 2-8 shows the display. (Alternatively, you can select a waveform from the list and drag it into the graph window.)

**Figure 2-8. Display of Time Domain Analysis**




   b. To zoom in on an area, click and hold the left mouse button to create a rectangular bounding box. You can stretch this box to surround the portion of the display you want to zoom.

c. To display a popup menu for zooming and placing waveform cursors, move the mouse cursor away from any portion of the waveform and click the right mouse button.

   You can use this menu to practice zooming the display and adding waveform cursors. Note that the **F5** key also creates waveform cursors. To delete a waveform cursor, click it and press **F5**.

d. To view the waveform properties, move the mouse cursor over any portion of the waveform, click the right mouse button and select **Properties** from the popup menu.

e. To delete a waveform from the display, click its name in the Waveform List pane and click the Delete icon in the toolbar.

3. Save the simulation results as a waveform database.

   a. In the  list, click the folder icon next to ex_rlc.1, which selects the results of this simulation as a database.

   b. Right-click to display a popup menu and click **Save As** to display the Save As dialog box.

   c. Click **Save** to save the current database of simulation results in the specified location.

4. Close the database.

   a. In the waveform list, click the folder icon next to ex_rlc.1.

   b. Right-click to display a popup menu.

   c. Click **Close** then **Yes** in the confirmation dialog box to close the display of ex_rlc.1.

## Frequency-domain analysis

The frequency domain analysis is a small-signal AC analysis that uses the values for ac_mag and ac_phase parameters of the input stimulus (v_pulse). This exercise uses the following default values for these parameters:

ac_mag=1.0
ac_phase=0.0

1. Run the simulation for frequency domain analysis.

   a. Return to the SystemVision window and select the following to display the Simulation Control dialog box:

      **Simulation > Simulate**

   b. In the **Simulations** tab, click the appropriate boxes to do the following:

Disable: Operating Point and Time-domain analysis
Enable: Frequency analysis

c. Under **Frequency Analysis**, type the following values:

**Freq Start** 10
**Freq Stop** 100k
**Setup > Number of Points** 10

Leave the settings on the other tabs as they are.

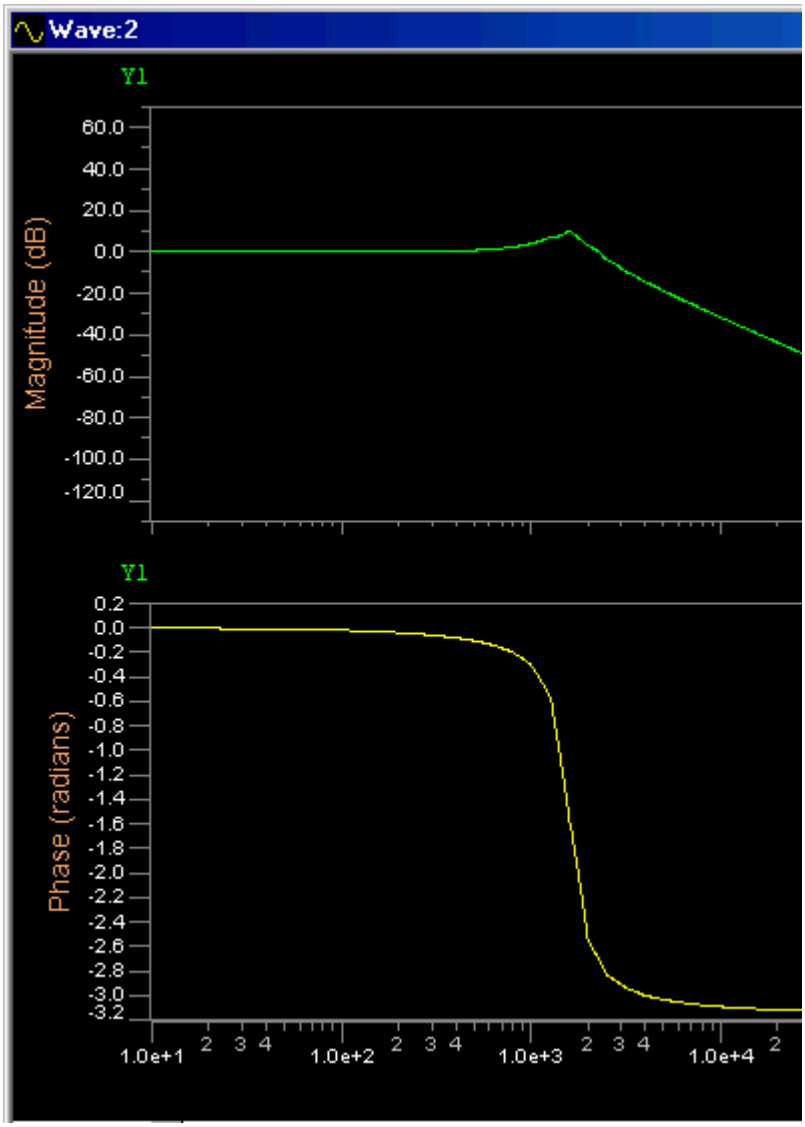
d. Click **OK**. This begins a frequency analysis on the active testbench. When simulation is complete, the waveform analyzer updates the waveform list to show the signals you can display for this analysis.

2. View results of the frequency analysis.

a. In the waveform list, find ex_rlc.2 and double-click vload.

Figure 2-9 shows the resulting waveforms for magnitude (in dB) and phase (in radians) vs. frequency (in Hz).

**Figure 2-9. Display of Frequency Analysis**




3. To save these results:
   a. In the signal list, click the folder icon next to ex_rlc.2, which selects the results of this simulation as a database.
   b. Right-click to display a popup menu.
   c. Select **Save As** to display the Save As dialog box.
   d. Click **Save** to save the current database of simulation results in the specified location.
4. Select **File** > **Exit** to quit the waveform analyzer.

## Parameter sweep (multi-run simulation)

With a SPICE-only or SPICE-on-top netlist, you can run multiple simulations on any model instance in a design using a specified set of parameter values. A different parameter value is used for each simulation until all values have been used. This is referred to as sweeping.

The following steps show how to create a SPICE-on-top netlist for the VHDL-AMS models in this example circuit and then perform a simulation sweep across a specified set of C1 capacitance values.

**Note**

VHDL-AMS instances in the netlist have the following restriction: only generics (parameters) that you have explicitly specified a value for can be swept. If you have not specified a value for a generic (that is, you are using the default value from the model), then that generic is not available for sweeping.

### Set up sweep parameters

Return to the SystemVision window and perform the following steps.

1. Netlist the schematic for ex_rlc as SPICE-on-top.
   a. Make sure the schematic is the active testbench.
   b. Select **Simulation > Testbench Options**.
   c. Set **Netlisting Option** as either:

      **Spice** or **Spice & VHDL**

   d. Set **Toplevel File Type** as **Spice**.
   e. Click **OK**.
   f. Select **Simulation > Netlist**.
2. Change simulation setup.
   a. Select **Simulation > Simulate**, which displays the Simulation Control dialog box.
   b. Click the **Simulations** tab and make the following changes:

      Enable Time Domain and Frequency analysis
      Disable Operating Point analysis if enabled
      Set the experiment name to ex_rlc_sweep.cmd
      Set the end time to 3ms

   c. Click the **Results** tab and select the following waveforms.

**NOTE:** For a SPICE netlist, waveform (signal) names associated with VHDL-AMS models have the letter “Y” appended as a prefix.

| | |
|---|---|
| V(vmid) | yl1 - S[i] |
| V(vinput) | yc1 - S[v] |
| V(vload) | yc1 - S[i] |
| yr1 - S[v] | yv_pulse1 - S[v] |
| yr1 - S[i] | yv_pulse1 - S[i] |
| yl1 - S[v] | |

In the **Results Database Name** field, type the following: ex_rlc_sweep

3. Specify a sweep parameter.
   a. Click the **Multi-Run** tab.
   b. In the **Parameter Change Type** dropdown list, select Sweep Values. This enables the Parameter Edit button.
   c. Click the **Parameter Edit** button.
   d. In the Sweep Parameter dialog box, click the browse button next to the Parameter field and select the following parameter from the list.

      yc1,cap

   e. Click **OK**
4. In the Sweep Parameter dialog box, specify the following:

   **Sweep Type** = Decade
   **Sweep Start** = 1e-5
   **Sweep End** = 1e-6
   **Steps per decade** = 4
5. Click **OK** to close the Sweep Parameter dialog box.

## Simulate and view results

1. Click **OK** in the Simulation Control dialog box to start the simulation.

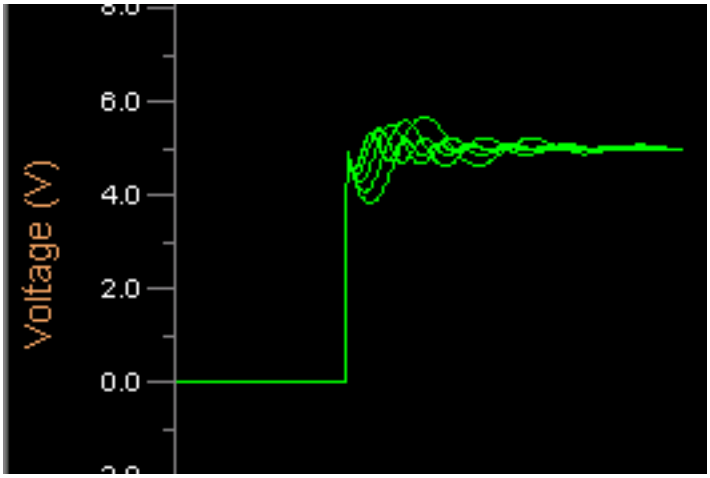
   **NOTE:** The status bar tracks the progress of each simulation run in the sweep (there should be five). The output log window displays a transcript of simulation activity.

   When simulations have been run for all parameter values, the SystemVision application launches the waveform analyzer.
2. In the waveform list, click [+] next to Time-domain Waveforms to expand the list of waveforms.

3. Look for the waveform named vmid. It should have a + on the waveform icon next to the name. This indicates multi-run results contained in a compound waveform.
4. Double-click vmid. This creates a display of waveforms for each simulation run.

   The display should resemble the multiple waveforms shown in Figure 2-10.

**Figure 2-10. Multi-run Results for Capacitance Sweep**




## End of Exercise

You have finished this exercise. Before exiting, you should do the following:

- In the waveform analyzer, close the display by selecting **Window > Close All** then **Yes**.
- In SystemVision, select **File > Close All** to close the project.

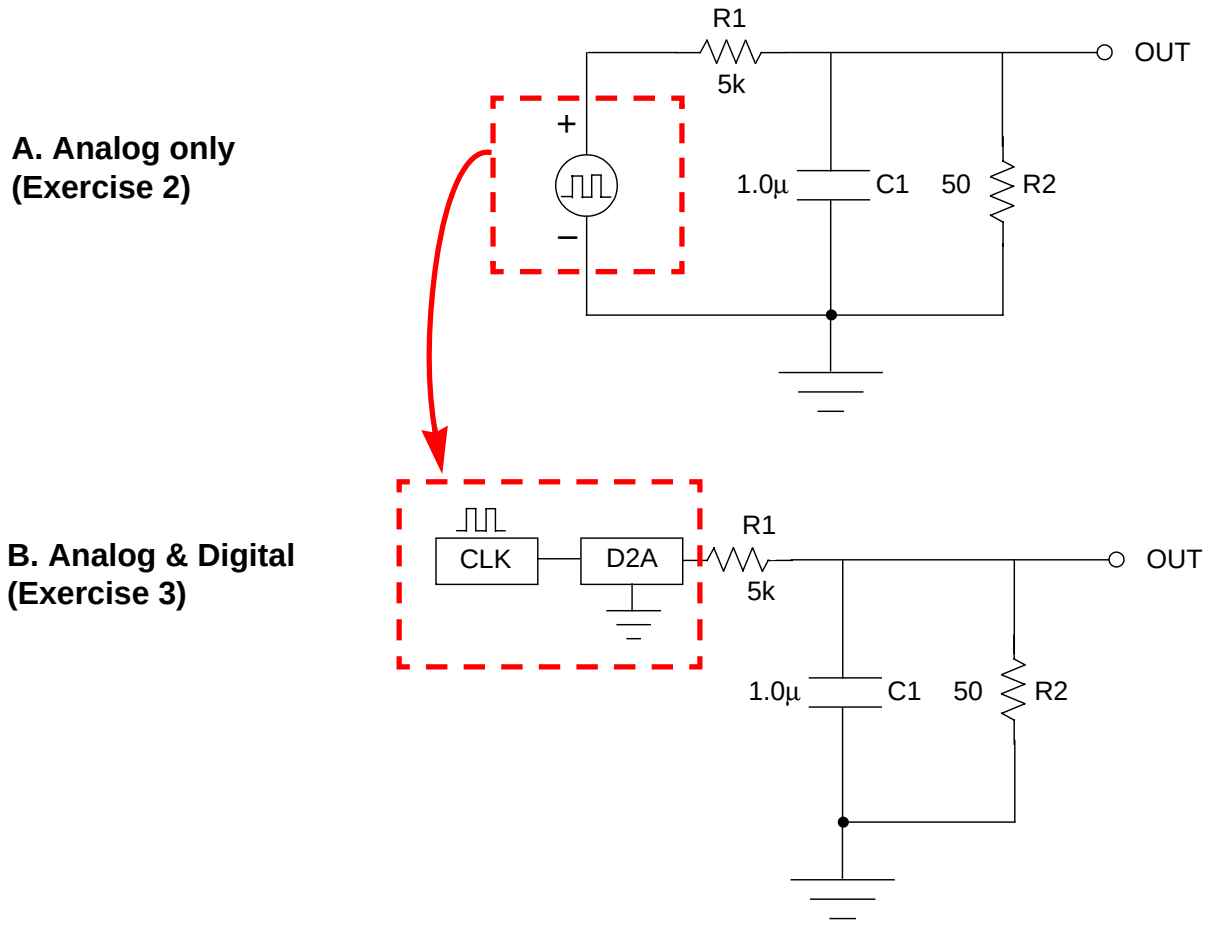
You can exit SystemVision and the waveform analyzer, or you can proceed to the exercise in the next chapter.

# Chapter 3
# Creating and Simulating a New Design

## Introduction

This chapter contains two exercises in which you create a simple electrical design and then make changes to it. In Exercise 2, you create an electrical circuit from analog models provided in the SystemVision library, simulate, and view the results. In Exercise 3, you replace the analog voltage source with a digital clock, resimulate the design, and view the results for essentially the same circuit, but one that uses a digital input stimulus. Figure 3-1 highlights the differences between the two designs.

**Figure 3-1. Changing circuit from analog-only to mixed-signal**



These exercises show you how to:

- Open a new project
- Create a schematic, using symbols and models from the Educational Library supplied with SystemVision
- Place and wire symbols
- Run a simulation and view results
- Change the design and resimulate

For basic information on how to use SystemVision™, refer to Chapter 1, “Overview”.

# Exercise 2: Create an Analog Design

This exercise shows how to create a new schematic for a design, save it as a project, simulate it, and view the simulation results.

## Open A New Project

1. If you do not have SystemVision running, invoke it as described in Chapter 1, Overview, “How to Invoke SystemVision”.
2. Select **File** > **New** from the menu bar:

   This displays the New dialog box.
3. Click the **Project** tab.
4. In the **Name** text field, type in a name for this project (such as “exercise2”). The name of a project must be an alphanumeric string with no spaces.
5. Click the **Browse** button next to the Location field. This displays the Choose folder dialog box. Navigate to a directory where you want to store the files and data for this project. Click **Select**.

   This returns to the New dialog box. Click **OK**.

## Create Schematic

1. To create a new schematic for the circuit in Figure 3-1, select **File** > **New**.
   a. In the New dialog box, click the **File** tab.
   b. From the Types pane on the right, select Schematic.
   c. In the **Name** text field, type in a name for this schematic (such as “ex2”).

d. Click **OK**.
This displays a blank schematic in the work area.

2. (Optional) To turn on or off the grid display, select **Project > Settings** from the main menu, click the **Project** tab, enable or disable **Grid**, and click **OK**.

## Place Symbols

1. Place a voltage source.

   a. Select **Add > Component** from the menu bar.

   This displays the Add Component dialog box.

   b. Select **Electrical > v_pulse.1 > Place** , using the indicated Directory, Symbol, and Button (you can ignore the number associated with the symbol name).

   Move the cursor into the schematic. This displays a small symbol for a voltage source in the schematic. Click to place the symbol.

2. Select and place the remaining symbols. As you did for the voltage source in the previous step, select component symbols from the Add Component dialog box and place them in the schematic window.

   a. Select **Electrical > resistor > Place** and place a resistor.

   b. Move the cursor back to the Add Component dialog box select Place to place another resistor symbol (R2).

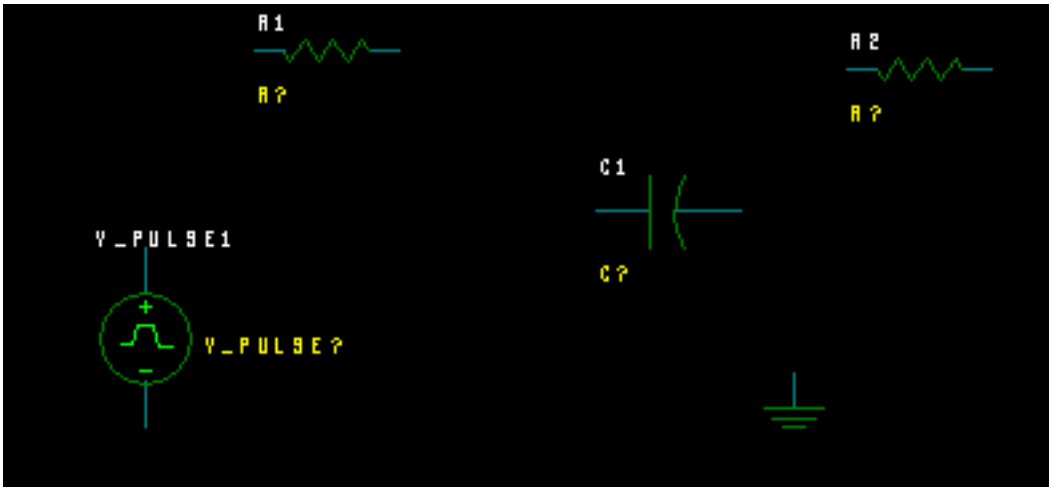
   c. Select **Electrical > capacitor > Place** and place a capacitor.

   d. Select **Electrical > electrical_ref > Place** and place an electrical ground symbol.

   e. Click **Close** in the Add Component dialog box.

   Figure 3-2 shows what the display looks like with the added components.

**Figure 3-2. Initial Placement of Symbols**




3. Position the symbols.

   a. Rotate C1 by right-clicking the symbol to display a popup menu. Select **Transform > Rotate CCW**.

      which rotates the capacitor symbol 90° counterclockwise.

   b. Repeat this rotation action on the symbol for R2.

   c. Select each symbol and move it into the positions shown in Figure 3-1.

## Wire Symbols

1. After you have moved the symbols into position, you need to connect them.

   a. From the menu bar, select **Add > Net**.

   b. Move the cursor to the left end of r1.

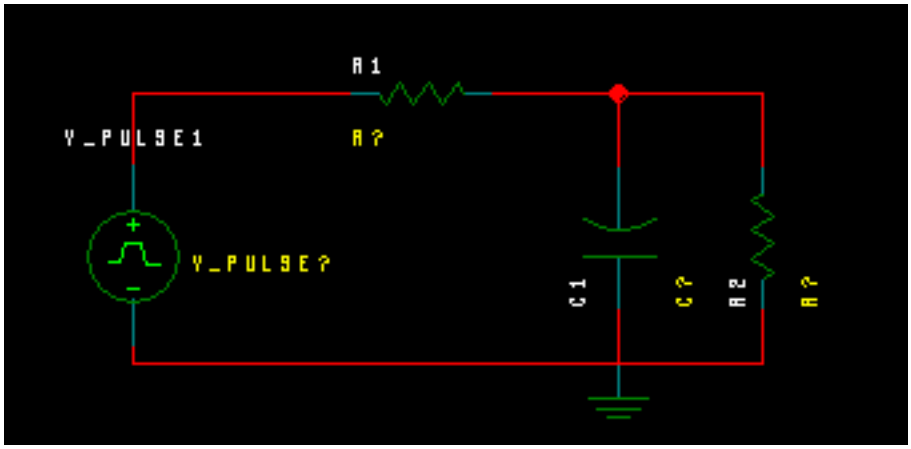
   c. Click and drag the cursor from r1 to the top connection point of v_pulse1.

      This inserts a net between those two symbols, which should follow at a right angle as you drag.

   d. Release the left mouse button. This completes the net between r1 and v_pulse1.

   e. Repeat this action to connect the remaining symbols. Figure 3-3 shows how the completed design should look.

**Figure 3-3. Completed Wiring**




2. Netlist the design and activate the testbench.
   a. Select **Simulation > Netlist** from the main menu.

      If necessary, answer yes to make this the active workbench.

   b. In the **Design Setup** tab of the Testbench Options dialog box, select the following:

      **Netlisting Option**: VHDL

   c. Click **OK**.

**Note**

If you see messages about wiring errors in the log window, you need to modify the wiring on your schematic to correct them and then rerun **Simulation > Netlist**.

3. Save the project. Select **File > Save**.

## Set Properties

1. Set the properties (parameter values) for voltage source v_pulse1.
   a. In the schematic work area, right-click the voltage source (v_pulse1). This displays a popup menu.

   b. Select **Edit Model Properties**, which displays the Model Properties dialog box.

   c. Click the **Parameters** tab. Note that the parameter names for this voltage source are listed in the left-hand column under Name.

   d. In the Value column, enter the following values for each indicated parameter:

| Name | Type | Default | Value |
|---|---|---|---|
| WIDTH | TIME | | 1 ms |

| Name | Type | Default | Value |
|---|---|---|---|
| PERIOD | TIME | | 2 ms |
| PULSE | VOLTAGE | | 5.0 |

WIDTH specifies a width of 1 ms for the output pulse.
PERIOD specifies a period of 2 ms for the entire pulse cycle (i.e., 50% duty cycle).
PULSE specifies an amplitude of 5.0 V for the output pulse.

e. Click **OK**.

2. Set properties (parameter values) for resistors r1 and r2.

   a. Right-click r1. Select **Edit Model Properties**, which displays the Model Properties dialog box.

   b. In the Model Properties dialog box, click the **Parameters** tab. Find the RES parameter in the Name column, move your cursor under the Value column, and click in the blank space. Type 5000 (or 5e3), which specifies 5 kΩ as the resistance for r1.

| Name | Type | Default | Value |
|---|---|---|---|
| RES | RESISTANCE | | 5000 |

   c. Click **OK**.

   d. Right-click r2 and select **Edit Model Properties**.

   e. In the Model Properties dialog box, click the **Parameters** tab.

   f. Find the RES parameter in the Name column, move the cursor under the Value column, and click in the blank space.

   g. Type 50, which specifies 50 Ω as the resistance for r2.

| Name | Type | Default | Value |
|---|---|---|---|
| RES | RESISTANCE | | 50 |

   h. Click **OK**.

3. Set properties (parameter values) for capacitor c1.

   a. Right-click c1 and select Edit Model Properties.

   b. In the Model Properties dialog box, click the **Parameters** tab.

   c. Find the CAP parameter in the Name column, move the cursor under the Value column, and click in the blank space.

d. Type 1e-6, which specifies 1.0µF as the capacitance for c1.

| Name | Type | Default | Value |
|---|---|---|---|
| CAP | CAPACITANCE | | 1e-6 |

e. Click **OK**.

4. Set properties for nets.

   a. Right-click the net (wire) between v_pulse1 and r1. Select **Properties**.

   b. In the Properties dialog box, click the **Name** tab.

   c. In the **Label** field, type VIN.

   d. Click **OK**.

   e. Right-click the wire between r1 and c1. Select **Properties**.

   f. In the Properties dialog box, click the **Name** tab.

   g. In the **Label** field, type VOUT.

   h. Click **OK**.

5. Save the schematic. Select **File > Save** from the main menu.

   This saves the schematic in the /sch directory of the Project directory you specified in Step 5 on page 34.

## Compile and Simulate

1. Under TestBenches in the Project Navigator **Simulation** tab, click the Project that contains the schematic you created and verify that it is the active testbench (the word [ACTIVE] should be next to it). If not, right-click and select **Set As Active Testbench**.

2. (Optional) Compile the design. Select **Simulation > Compile > Compile All**. The output log window displays a transcript of the compilation.

   Because SystemVision performs all necessary compilation for the active testbench at simulation, you can choose to skip this step.

3. Select **Simulation > Simulate** from the menu.

   which displays the Simulation Control dialog box (shown in Figure 2-4).

4. In the **Simulations** tab, make the following selections:

   a. Enable: Operating Point and Time-Domain analysis

   b. Under **Time-Domain Analysis**, enter the following value:
   **End Time**: 0.5

5. Click the **Results** tab, and do the following:

   i. Click the arrow for the dropdown list under **Time-domain Analysis** and select Selected Waveforms.

   ii. Display the list of available waveforms to select by clicking on the browse button next to this field:

   iii. In the Waveform List dialog box, click **Clear All**.

   iv. Select the check boxes for the following Waveforms:

| | |
|---|---|
| V(vin) | r1 - S[i] |
| V(vout) | r2 - S[v] |
| v_pulse1 - S[v] | r2 - S[i] |
| v_pulse1 - S[i] | c1 - S[v] |
| r1 - S[v] | c1 - S[i] |

   v. Click **OK** to close the Waveform List dialog box.

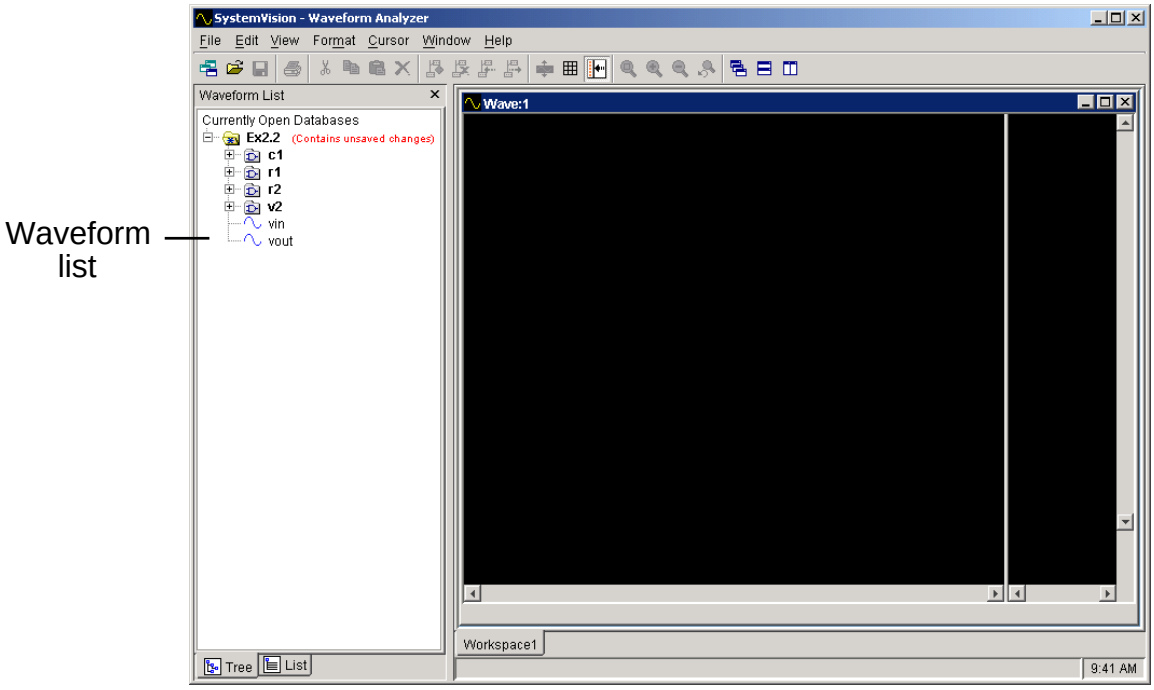
6. To simulate, click **OK** in the Simulation Control dialog box.

   This runs a simulation on the active testbench selected in the Project Navigator. When the simulation completes, SystemVision launches the waveform analyzer.

## View results

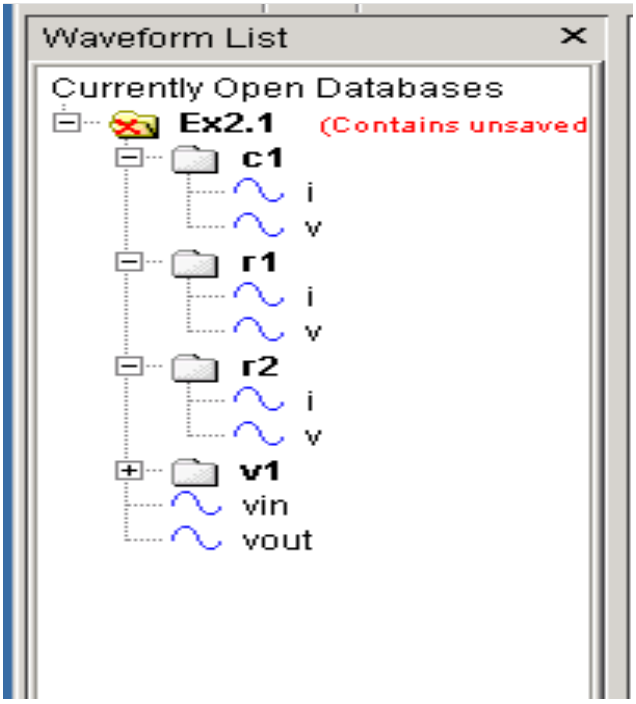
Figure 3-4 shows how the waveform analyzer should look when SystemVision finishes simulation (your display may vary slightly).

**Figure 3-4. Waveform Analyzer Display**




1. In the waveform list window, click the [+] indicators next to c1, r1, and r2 to expand the list of waveform names for each component. Figure 3-5 shows what the waveform list should look like.

**Figure 3-5. Expanded Waveform List**



2. Display the following waveforms by double-clicking (or by dragging-and-dropping them into the waveform display pane; be sure to drag them each below the other).

   Under c1: i, v
   Under r1: v
   Under r2: v

   Note that the horizontal display for each waveform is quite compressed—to better view each waveform, you need to change the range of the X-axis.

   You can change the range of the X-axis either by clicking and dragging the mouse cursor across the time values or by changing X-axis properties, as described in the next step.

3. Change X-Axis Properties.

   a. Move the mouse cursor over the word Time along the X-axis and right-click.

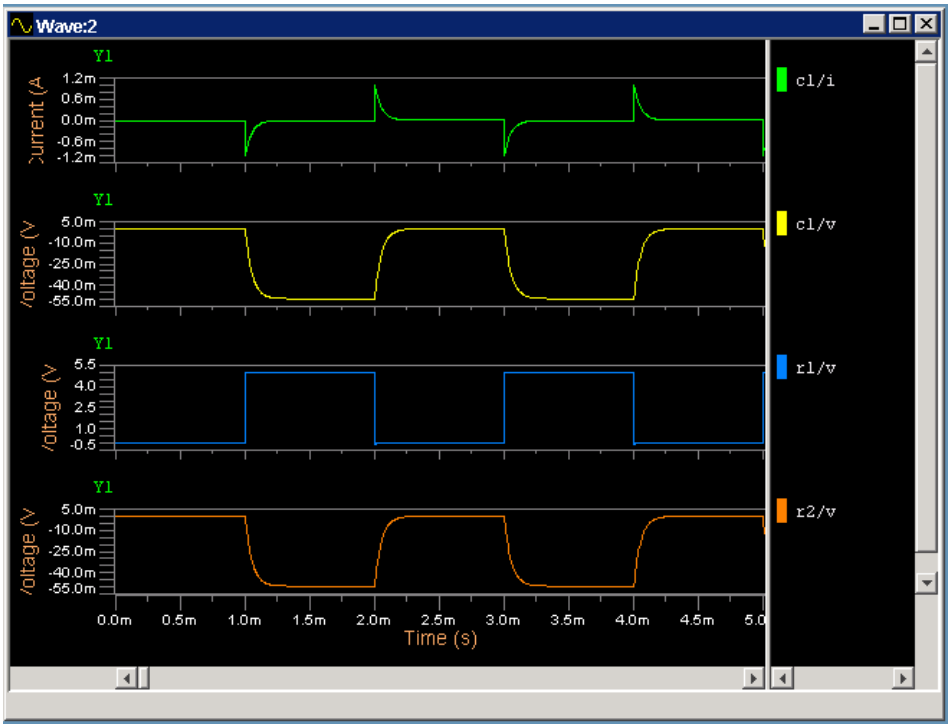
   b. In the popup menu, select **Properties**. This displays the X-Axis Properties dialog box.

   c. Under **Axis Range**, disable **Auto Range**. Set **Max** to 0.005.

   d. Click **OK**.

4. Figure 3-6 shows the four waveforms that should appear in the workspace. Note the current and voltage values for c1.

**Figure 3-6. Pulse Behavior From Analog Source**



5. Save the waveform database.
   a. From the menu bar, select **File > Save**, which displays the Save Window dialog box that prompts you for a file name.
   b. In the File name field, type src_analog.
   c. Click **Save**.
6. Close all waveform databases.
   a. In the Waveform List window, right-click Currently Open Databases.
   b. In the Waveform List popup menu, select **Close All Databases**.
   c. In the Confirm dialog box, click **Yes**.
7. Return to the SystemVision window for Exercise 3.

# Exercise 3: Create a Mixed-Signal Design

This exercise shows how to swap out an analog model for an equivalent digital model, re-simulate, and view results. Note that this mixed-signal design requires that you insert a special digital-to-analog interface model.

## Create a New Project

1. In the Project Navigator **Simulation** tab, right-click the active testbench (ex2).
2. Select **Remove Testbench** from the popup menu. Click **Yes** in the dialog box that is displayed.
3. Select **File > New** from the main menu to display the New dialog box.
4. Click the **Project** tab.
5. Click the **Browse** button to navigate to location where you want to store this project.
6. In the **Name** field, enter a unique name for a new project, such as “exercise3”.
7. Click **OK**. Click **Yes** in the dialog box that is displayed (which closes the current project for Exercise 2).

   This changes the displayed project from exercise2 to the Welcome screen.

## Copy Schematic File

**Note**

In SystemVision, you cannot copy and paste between schematics that are in different projects. However, you can copy a schematic file from a project folder in Windows, paste it to the folder (directory) of a different project, and then open the schematic in that project.

1. In Windows Explorer, navigate to C:\Mentor_Projects or the folder where you saved the project for Exercise 2 (the project directory you specified in Step 5 on page 34).
2. Navigate to the exercise2\sch folder.
3. Select the schematic file you created in Exercise 2.
4. From the Explorer menu bar, select **Edit > Copy.**
5. Navigate to the \sch folder of the project directory for Exercise 3 that you specified in Step 5, above.
6. Select **Edit > Paste.**
7. Select the schematic file and rename it to “ex3.1”.

## Open New Schematic

1. In the Project Navigator, select the **Project** tab.
2. Click [+] next to the Design Roots listing. The schematic copied from Exercise 2 should be listed as “ex3”.
3. Click ex3. This displays the circuit from Exercise 2.
4. Select **File > Save**.

## Replace Analog Source with Digital Source

1. Select the voltage source (v_pulse1).
2. Delete the voltage source. Select **Edit > Delete** from the main menu (or press the Delete key).
3. Place a digital clock symbol into the schematic.
   a. Select **Add > Component** from the menu bar.

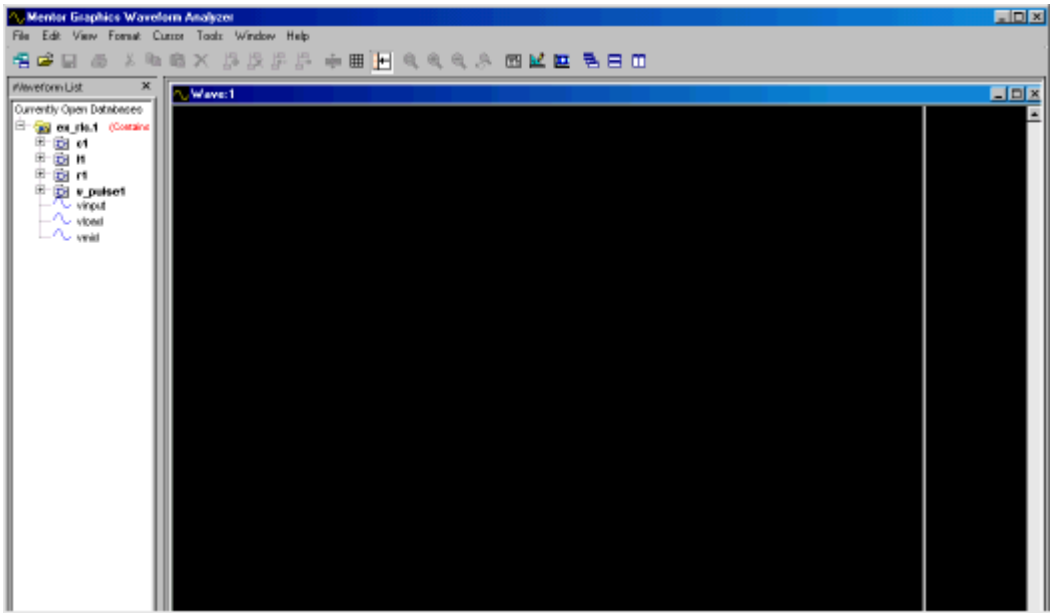
      This displays the Add Component dialog box.

   b. Select Digital from the list of directories, select clock.1 from the list of Symbols, then click **Place** (you can ignore the number associated with the symbol name).

This displays a small symbol for a clock.
Move the cursor to the schematic work area and click to place the symbol.

4. Select the MixedSignal directory in the Add Component dialog box.
5. Select and place a one-bit digital-to-analog symbol (d2a_bit.1).
6. Close the Add Component dialog box.
7. Move the symbols and wires around as needed so you can wire the clock to the d2a and the d2a to r1. Note that the ground symbol needs to connect only to r2 and c1. Figure 3-7 shows the new design.

**Figure 3-7. Mixed-Signal Circuit**




## Specify Parameter Values

1. Click the d2a_bit symbol and verify its parameter values. This symbol represents an ideal, one-bit digital-to-analog converter that converts the digital clock signal to an analog voltage.
   a. Right-click the symbol and select **Edit Model Properties**.
   b. In the Model Properties dialog box, note the following parameters and their default values for analog output.

| Name | Type | Default | Value |
|---|---|---|---|
| VHIGH | VOLTAGE | 5.0 | |
| T_RAMP | REAL | 1.0E-9 | |

| Name | Type | Default | Value |
|---|---|---|---|
| VLOW | VOLTAGE | 0.0 | |

c. Click **Cancel** to use the default values for the d2a_bit converter.

2. Click the clock symbol and specify its parameter values.

   a. Right-click the symbol and select **Edit Model Properties**.

   b. In the Model Properties dialog box, note the following clock parameters (the duty cycle parameter has a default of value of 0.5, or 50%, which emulates the analog pulse from Exercise 2).

   c. Specify a period of 2 ms, as shown.

| Name | Type | Default | Value |
|---|---|---|---|
| PERIOD | TIME | | 2 MS |
| DUTY | REAL | 0.5 | |

   d. Click **OK**.

3. Netlist the design and activate the testbench.

   a. Select **Simulation > Netlist** from the main menu.

   If necessary, answer **Yes** in the confirmation dialog box.

   b. In the Testbench Options dialog box, select the following:

   **Netlisting Option**: VHDL

   c. Click **OK**.

**Note**

If you see messages about wiring errors in the log window, you need to modify the wiring on your schematic to correct them and then rerun **Simulation > Netlist**.

4. Save this schematic by choosing **File > Save** from the menu bar.

## Simulate

1. Select **Simulation > Simulate** from the menu bar.

   which displays the Simulation Control dialog box (as shown in Figure 2-4).

2. In the **Simulations** tab, make the following selections:

   a. Enable: **Operating Point Analysis**, **Time-Domain Analysis**

b. Under **Time-Domain Analysis**, enter the following value:
**End Time**: 0.5

3. Click the **Results** tab, and do the following:

   i. Click the arrow for the dropdown list under **Time-domain Waveforms** and select Selected Waveforms.

   ii. Display the list of available waveforms to select by clicking on the browse button next to this field:


   iii. In the Waveform List dialog box, click **Clear All**.

   iv. Select the check boxes for the following waveforms:

| | |
|---|---|
| r1 - S[v] | r2 - S[v] |
| r1 - S[i] | r2 - S[i] |
| d2a_bit1 - S[vout] | c1 - S[v] |
| d2a_bit1 - S[iout] | c1 - S[i] |

   v. Click **OK** to close the Waveform List dialog box.

4. To simulate, click **OK** in the Simulation Control dialog box.

   This runs a simulation on the active testbench selected in the Project Navigator. When the simulation completes, SystemVision launches the waveform analyzer.

## View Results

1. In the Waveform List window of the Waveform Analyzer, click the [+] next to c1, r1, and r2 to expand the list of waveforms below these components.

2. Display the following waveforms by double-clicking (or by dragging-and-dropping them into the waveform display pane):

   Under c1: i, v
   Under r1: v
   Under r2: v

   Note that the display for each waveform is quite compressed—to better view each waveform, you need to change the range of the X-axis. You can change the range of the X-axis either by clicking and dragging the mouse cursor across the time values or by changing the X-axis properties.

   Figure 3-8 shows the four waveforms that should appear in the workspace. Note the current and voltage values for c1.

3. Save this database.

a. From the menu bar, select **File > Save**, which displays the Save Window dialog box that prompts you for a file name.

b. In the **File name** field, type src_digital.

c. Click **Save**.

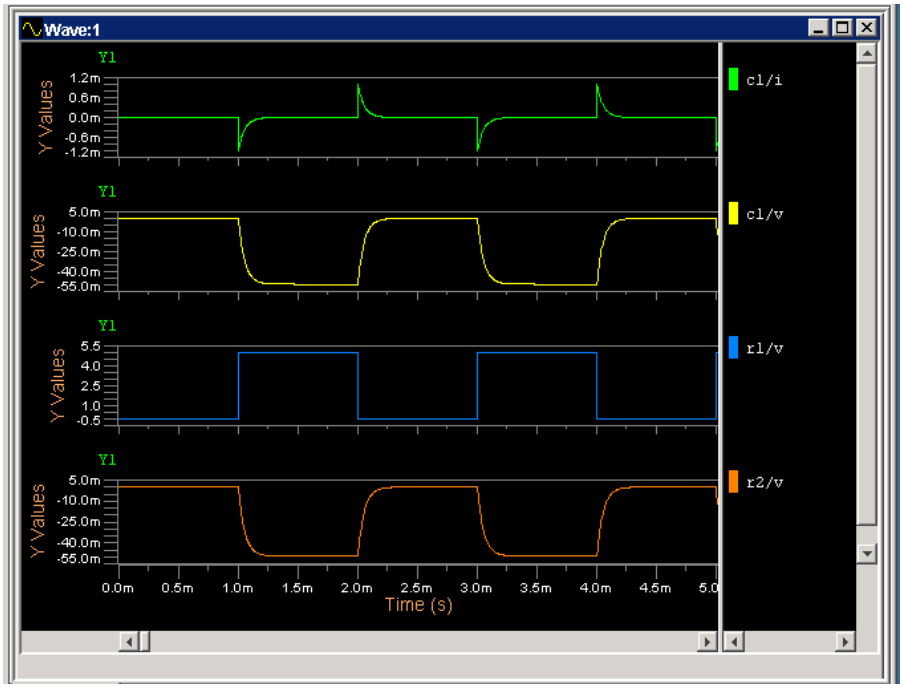
4. Close all waveform databases.

a. In the Waveform List window, right-click Currently Open Databases.

b. In the Waveform List popup menu, select **Close All Databases**.

c. In the Confirm dialog box, click **Yes**.

**Figure 3-8. Pulse Behavior From Digital Clock**



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